HEWLETT-PACKARD COMPANY
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PATENT APPLICATION

ATTORNEY DOCKET NO. 10001459-1

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IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Michael R. Krause et al. **Confirmation No.:** 2070

Application No.: 09/783,159 **Examiner:** T. M. Bonura

Filing Date: Feb. 13, 2001 **Group Art Unit:** 2114

Title: HIGHLY AVAILABLE, MONOTONIC INCREASING SEQUENCE NUMBER GENERATION

Mail Stop Appeal Brief-Patents
Commissioner For Patents
PO Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL OF APPEAL BRIEF

Sir:

Transmitted herewith is the Appeal Brief in this application with respect to the Notice of Appeal filed on **Dec. 9, 2004**.

The fee for filing this Appeal Brief is (37 CFR 1.17(c)) $500.00.

(complete (a) or (b) as applicable)

The proceedings herein are for a patent application and the provisions of 37 CFR 1.136(a) apply.

( ) (a) Applicant petitions for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)-(d) for the total number of months checked below:

( )	one month	$120.00
( )	two months	$450.00
( )	three months	$1020.00
( )	four months	$1590.00

( ) The extension fee has already been filled in this application.

(X) (b) Applicant believes that no extension of time is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

Please charge to Deposit Account **08-2025** the sum of **$500.00**. At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account 08-2025 pursuant to 37 CFR 1.25. Additionally please charge any fees to Deposit Account 08-2025 under 37 CFR 1.16 through 1.21 inclusive, and any other sections in Title 37 of the Code of Federal Regulations that may regulate fees. A duplicate copy of this sheet is enclosed.

(X) I hereby certify that this correspondence is being deposited with the U.S. Postal Service as Express Mail, Airbill No. EV375345604US, in an envelope addressed to: MS Appeal Brief - Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Date of Deposit: February 9, 2005

Typed Name: **June Nguyen**

Signature: June Nguyen

Respectfully submitted,

Michael R. Krause et al.

By _____

Michael A. Papalas

Attorney/Agent for Applicant(s)
Reg. No. **40,381**

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HEWLETT-PACKARD COMPANY
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P.O. Box 272400
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Docket No.: 10001459-1
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Michael R. Krause et al.

Application No.: 09/783,159 Confirmation No.: 2070

Filed: February 13, 2001 Art Unit: 2114

For: HIGHLY AVAILABLE, MONOTONIC INCREASING SEQUENCE NUMBER GENERATION Examiner: T. M. Bonura

APPEAL BRIEF

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

As required under § 41.37(a), this brief is filed within two months of the Notice of Appeal filed in this case on December 9, 2004, and is in furtherance of said Notice of Appeal.

The fees required under § 41.20(b)(2), and any required petition for extension of time for filing this brief and fees therefor, are dealt with in the accompanying TRANSMITTAL OF APPEAL BRIEF.

This brief contains items under the following headings as required by 37 C.F.R. § 41.37 and M.P.E.P. § 1206:

I. Real Party In Interest
II Related Appeals and Interferences
III. Status of Claims
IV. Status of Amendments
V. Summary of Claimed Subject Matter

I. REAL PARTY IN INTEREST

The real party in interest for this appeal is: Hewlett-Packard Development Company, L.P., a Texas Limited Liability Partnership having its principal place of business in Houston, Texas.

II. RELATED APPEALS, INTERFERENCES, AND JUDICIAL PROCEEDINGS

There are no other appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

A. Total Number of Claims in Application

There are 23 claims pending in application, currently identified as 1-16, and 21-27.

B. Current Status of Claims

1. Claims canceled: 17-20
2. Claims withdrawn from consideration but not canceled: None
3. Claims pending: 1-16 and 21-27
4. Claims allowed: 21-27
5. Claims rejected: 1, 10, 15 and 16
6. Claims objected to: 2-9 and 11-14

C. Claims On Appeal

The claims on appeal are claims 1-16.

IV. STATUS OF AMENDMENTS

All amendments have been entered.

V. SUMMARY OF CLAIMED SUBJECT MATTER

Information systems assign a sequence of ever-increasing (monotonic) numbers to database actions, so that the order of these transactions may be retained and the processing of the actions may occur in an ordered manner. Although relatively simple to implement in a single processor system, to be practical, a sequence numbering application should be scalable, i.e. capable of being employed among an arbitrary number of logical nodes distributed across a communication medium or system fabric. (*See* Application p. 2)

Embodiments of the present invention provide monotonic sequence number generation by establishing a primary and a secondary generator. (*See* Application p. 4 and FIGURE 4) Applications that utilize transaction numbering to order data may initiate a call in software to obtain a sequence number. (*See* Application p. 4 and FIGURE 4) The software call utilizes an interface to bypass ordinary network or communication channel protocols. (*See* Application p. 4 and FIGURE 4) The interface, defined by a hardware or firmware implementation device, generates a sequence number request to the primary generator. (*See* Application p. 4 and FIGURE 4) After receiving the sequence number request, the primary sequence number generator determines the appropriate sequence number in a monotonic manner. (*See* Application p. 4 and FIGURE 4) The primary sequence number updates its memory to reflect that the determined sequence number has been utilized, and forwards the determined sequence number to the secondary sequence number generator. (*See* Application p. 4 and FIGURE 4) The secondary sequence number generator updates its memory to reflect that the determined sequence number has been utilized, and forwards the determined sequence number to the initial hardware implementation device. (*See* Application p. 4 and FIGURE 4) If the primary generator becomes unavailable, then the underlying architecture of preferred embodiments of the present invention reassign the secondary generator as the primary generator and assign a new secondary generator. (*See* Application p. 4 and FIGURE 4)

Embodiments of the present invention may be arranged as sequence number generation systems that provide monotonic sequence numbers that include a plurality of

sequence number devices, connected via a fabric, including at least a primary sequence number generator and a secondary sequence number generator. (*See* Application p. 9 and FIGURE 2). The primary sequence number generator is typically disposed to receive a sequence number request from an originating device and to forward a sequence number response to the secondary sequence number generator. (*See* Application p. 9 and FIGURE 2). The secondary sequence number generator is typically disposed to receive the sequence number response, to store the sequence number response in memory, and to forward the response to the originating device. (*See* Application p. 9 and FIGURE 2). The primary and secondary sequence number generators store current sequence numbers in memory associated with respective host processor systems via direct memory access operations. (*See* Application p. 13). In addition, the sequence number requests are often associated with a pipeline of sequence number requests form the originating device. (*See* Application p. 14).

VI. GROUNDS OF REJECTION/OBJECTION TO BE REVIEWED ON APPEAL

A. Claims 1, 10, 15, and 16 stand rejected under 35 U.S.C. § 103(a) in light of the combination of *Hill* and *Chan*.

B. Claims 2-9 and 11-14 stand objected to as depending from rejected claims.

VII. ARGUMENT

A. Claims 1, 10, 15, and 16 stand rejected under 35 U.S.C. § 103(a) in light of the combination of *Hill* and *Chan*.

The Examiner has rejected claims 1, 10, 15, and 16 as obvious in light of Hill et al., U.S. Patent No. 6,161,198 (hereinafter *Hill*) and Chan, U.S. Patent No. 6,539,446 (hereinafter *Chan*). The Appellant respectfully maintains, however, that the Examiner has yet to establish a prima facie case for rejecting these claims. The Examiner is required to meet three basic criteria in order to establish a prima facie case. *See In re Vaeck*, 947 F.2d 488 (Fed. Cir. 1991). First, the Examiner must recite a motivation for combining the references proposed that is either found in the references themselves or that was generally known to those of ordinary skill in the art at the time the invention was made. Second, the combination proposed must have inspired a reasonable expectation of success. Third, the combination must teach or suggest each and every limitation of the rejected claims. Without conceding that the Examiner has established the second criteria, the Appellant respectfully asserts no

motivation exists for combining *Hill* and *Chan* as the Examiner desires, and that even when combined, the proposed references do not teach or suggest each and every limitation of the claims rejected.

1. No motivation exists for combining *Hill* and *Chan*.

In the Office Action mailed August 9, 2004 (hereinafter "Final Action"), the Examiner contends that *Chan* "discloses a system wherein lock data is generated for a first node and can be passed to a second node." *See* Final Action at 3. The Examiner then concludes that it would be obvious to one of ordinary skill in the art to modify *Hill*, which "does not disclose a system that the first generator forwards the sequence number to the second generator," *Id* at 3, with the teachings of *Chan* in order to "achieve a sequence number passing system in which the sequence number is available if the node fails." *Id* at 3. The Appellant disagrees, and respectfully points out that one of *Hill's* principle features is to "provide a system for providing transaction indivisibility," *see Hill* at column 1 lines 50-51. This is accomplished, in part, by comparing the sequence numbers of messages transmitted from recovered host. *See Id* at column 9 line 60 – column 10 line 7. By comparing the sequence number of the re-transmitted message to the sequence number expected, *Hill* ostensibly "provides a convenient and accurate method of maintaining indivisibility." *Id* at column 10 lines 8-9. Thus, if one were to modify *Hill* by adding features of *Chan* that ensure the correct order of sequence numbers are followed when a node fails, the sequence number would always be that which was expected when the node recovers. The Federal Circuit has determined that "if [a] proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification." In *In re Rouffet*, 149 F.3d 1350, 1357 (Fed. Cir. 1998). Combining the *Hill* and *Chan* as the Examiner desires would render *Hill's* sequence number comparison meaningless, and render the features of *Hill* that ensure indivisibility unsatisfactory for their intended purpose. Therefore, no motivation exists for the proposed combination, and the Appellant respectfully asks this Board to reverse the 35 U.S.C. § 103(a) rejection of claims 1, 10, 15, and 16.

2. The Examiner's proposed combination does not teach or suggest all of the limitations of Claim 1.

Even if combined, however, the proposed combination still can not establish a prima facie case. In the Final Action, the Examiner rejected claim 1 as obvious in light of the combination of *Hill* and *Chan*. In making this rejection, the Examiner relied on *Hill* remarking that "[r]egarding the limitation of, 'generating a sequence number at an originating node,' Hill discloses a system wherein a processing unit transmits a message and includes a sequence number." *See* Final Action at 3. In the Response dated October 5 (hereinafter "Response to Final"), the Appellant pointed out that the Examiner had misunderstood the limitations of claim 1, which actually recites "generating a sequence number request at an originating node." Thus, even when accepted as true, the Examiner's representations of the teachings of the *Hill* and *Chan* could not establish a prima facie case of obviousness. In the Advisory Action dated November 10, 2004, rather than clarify his position, the Examiner merely stated that the Appellant's arguments were unpersuasive. Such a contention, however, does not establish the criteria of a prima facie case.

"The examiner bears the initial burden of factually supporting any *prima facie* conclusion of obviousness. If the examiner does not produce a *prima facie* case, the Appellant is under no obligation to submit evidence of nonobviousness." *See eg. In re Rinehart*, 531 F.2d 1048 (CCPA 1976), and *In re Saunders*, 444 F.2d 599 (CCPA 1971). In order to establish a prima facie case, the Examiner must show, among other things, that the proposed combination teaches or suggests each and every limitation of a rejected claim. Claim 1 of the present application requires "generating a sequence number request at an originating node." The Examiner has yet to even contend that the combination of *Hill* and *Chan* teaches or suggests this limitation. Therefore, a prima facie case has never been established for rejecting claim 1, and the Appellant respectfully asks this Board to reverse the 35 U.S.C. § 103(a) rejection.

Further, the Appellant respectfully submits that the Examiner's misunderstanding of the limitations of claim 1 has lead to a proposed combination that can never establish a prima facie case. The Examiner has described *Hill* as disclosing "a system wherein a processing unit transmits a message and includes a sequence number." *See* Final Action page 3 (citing *Hill* column 2, lines 6-8). The system of *Hill*, as depicted in figure 5 and as described by the Examiner, seems to have each originating node generate its own sequence number. Claim 1,

in contrast, is a method requiring "generating a sequence number request at an originating node," where the sequence number itself generated elsewhere. Thus, when correctly recited, it is clear that the concepts encapsulated by claim 1 are fundamentally different than those taught or suggested by *Hill*. Because *Chan* does not teach or suggest the missing limitations either, the Appellant respectfully submits that the proposed combination can not establish a prima facie case for rejecting claim 1. Thus, the Appellant respectfully asks this Board to reverse the 35 U.S.C. § 103(a) rejection of claim 1.

3. The Examiner's Proposed Combination Does Not Establish a Prima Facie Case For Rejecting Claim 10.

The Examiner also appears to be mistaken with regard to the limitations of claim 10. In the response to the first Office Action, dated February 26, 2004 (hereinafter "First Response"), the Appellant demonstrated that *Hill* does not teach or suggest a sequence number generator disposed to receive a sequence number request from an originating device, as required by claim 10. *See* First Response page 10. In the Final Action, the Examiner responded by contending that "Hill discloses that a sequence number can be generated by a host along with a message to be sent and then the message and the number can be received with the message from the corresponding host." Final action page 7 (citing Figure 6 and column 8, lines 45-62). In the Response to Final, the Appellant pointed out that this contention appeared to misstate the limitations of claim 10, which, requires a "sequence number generator disposed to receive a sequence number request from an originating device," not a device that generates its own sequence number. Rather than adjust the rejection to properly establish a prima facie case in the Advisory Action, however, the Examiner merely stated that the Appellant's arguments were unpersuasive.

Again, a prima facie case can only be established when, among other things, the Examiner demonstrates that the proposed combination teaches or suggests each and every limitation of the rejected claim. In rejecting claim 10, the Examiner insists that *Hill* teaches that a "sequence number can be generated by a host along with a message to be sent and then the message and the number can be received with the message from the corresponding host." The system of *Hill*, as depicted in figures 5 and 6 and as described by the Examiner, seems to have each originating host generate its own sequence number. Claim 10, in contrast, requires a "sequence number generator disposed to receive a sequence number request from an

originating device," where the sequence number response comes from the primary sequence number generator. Thus, when properly recited, the concepts of claim 10 are fundamentally different than those taught or suggested by *Hill*. Because *Chan* does not teach or suggest the missing limitations either, the Appellant respectfully submits that the proposed combination can not establish a prima facie case for rejecting claim 10. Therefore, the Appellant respectfully asks this Board to reverse the 35 U.S.C. § 103(a) rejection of claim 10.

4. The Examiner's proposed combination does not establish a prima facie case for rejecting claims 15 and 16.

Claims 15 and 16 depend indirectly from claim 10, and thus inherit all of that claim's limitations. Although both claims 15 and 16 recite limitations that make them patentable in their own right, each is at least patentable for depending from a patentable base claim. Therefore, the Appellant respectfully asks the Board to reverse the 35 § 103(a) rejection of claims 15 and 16 as well.

B. Claims 2-9 and 11-14 stand objected to as depending from rejected claims.

Claims 2-9 depend either directly or indirectly from claim 1, and claims 11-14 depend either directly or indirectly from claim 10. As demonstrated above, claim 1 and claim 10 are patentable over the prior art of record. Therefore, the objections to claims 2-9 and 11-14 are moot, and the Appellant respectfully asks that they be withdrawn.

VIII. CLAIMS

A copy of the claims involved in the present appeal is attached hereto as Appendix A. As indicated above, the claims in Appendix A include the amendment filed by Appellant on October 5, 2004.

IX. EVIDENCE

No evidence pursuant to §§ 1.130, 1.131, or 1.132 or entered by or relied upon by the Examiner is being submitted.

X. RELATED PROCEEDINGS

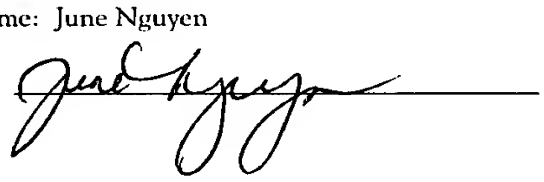
No related proceedings are referenced in II. above, or copies of decisions in related proceedings are not provided, hence no Appendix is included.

The fees required under § 41.20(b)(2), and any required petition for extension of time for filing this brief and fees therefor, are dealt with in the accompanying TRANSMITTAL OF APPEAL BRIEF. Appellant believes no additional fee is due with this response. However, if an additional fee is due, please charge our Deposit Account No. 08-2025, under Order No. 10001459-1 from which the undersigned is authorized to draw.

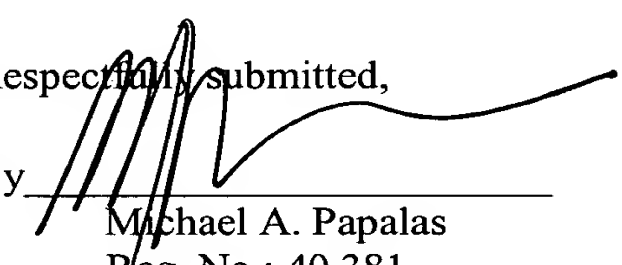
I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as Express Mail, Airbill No. EV375345604US in an envelope addressed to: MS Appeal Brief - Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Date of Deposit: February 9, 2005

Typed Name: June Nguyen

Signature: 

Respectfully submitted,

By 

Michael A. Papalas
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APPENDIX A

Claims Involved in the Appeal of Application Serial No. 09/783,159

1. (Previously Presented) A method of providing monotonic sequence number, comprising the steps of:

(a) establishing a primary sequence number generator;

(b) establishing a secondary sequence number generator;

(c) generating a sequence number request at an originating node;

(d) forwarding the sequence number request to the primary sequence number generator;

(e) forwarding a sequence number response to the secondary sequence number generator;

(f) storing the sequence number response at the secondary sequence number generator; and

(g) forwarding the response sequence number from the secondary sequence number generator to the originating node.

2. (Original) The method of claim 1, wherein step (c) comprises the sub-steps of:

performing a sequence number request call by a software process operating upon a host processor system to a user-space function; and

executing a sequence number request via an interface located at the originating node.

3. (Original) The method of claim 2 further comprising the step of:

receiving the sequence number response at the interface; and

communicating the sequence number response to the software process.

4. (Original) The method of claim 3, wherein the software process executes a spin loop while waiting to receive the sequence number response.

5. (Original) The method of claim 4, wherein the software process is placed into a sleep state if the sequence number response is not received within a predetermined amount of time.

6. (Original) The method of claim 2, wherein the interface is a hardware card linked to a sequence number fabric.

7. (Original) The method of claim 6, wherein the host processor system comprises a second hardware card linked to a duplicate sequence number fabric.

8. (Previously Presented) The method of claim 2, wherein the primary and secondary sequence number generators store current sequence numbers in memory associated with respective host processor systems via direct memory access operations.

9. (Previously Presented) The method of claim 6, wherein the hardware card pipelines a plurality of sequence number requests.

10. (Previously Presented) A sequence number generation system for providing monotonic sequence numbers, comprising:

a plurality of sequence number devices, connected via a fabric, including at least a primary sequence number generator and a secondary sequence number generator;

the primary sequence number generator disposed to receive a sequence number request from an originating device and to a forward sequence number response to the secondary sequence number generator; and

the secondary sequence number generator disposed to receive the sequence number response, store the sequence number response in memory, and forward the response to the originating device.

11. (Previously Presented) The system of claim 10, wherein each sequence number device includes lower level sequence number routines accessible by software processes operating on a host processor system via user-space functions.

12. (Original) The system of claim 11, wherein the user-space functions includes a request new sequence number function.

13. (Original) The system of claim 12, wherein the request new sequence number function causes a requesting application process to execute a spin loop while waiting for receipt of a new sequence number.

14. (Original) The system of claim 13, wherein the requesting application process is placed in a sleep state if the new sequence number is not received within a predetermined amount of time.

15. (Original) The system of claim 10, wherein the primary and secondary sequence number generators store current sequence numbers in memory associated with respective host processor systems via direct memory access operations.

16. (Original) The system of claim 10, wherein the sequence number request is associated with a pipeline of sequence number requests form the originating device.

17-20. (Canceled)

21. (Previously Presented) A distributed computing system, comprising:

a plurality of nodes that each comprise at least one processor and at least one sequence number device;

a fabric interconnecting said sequence number devices of said plurality of nodes;

wherein a respective application is executed on a processor of each of said plurality of nodes that uses sequence numbers issued monotonically within said plurality of nodes and said sequence number devices of said plurality of nodes comprises a primary sequence number generator and a secondary sequence number generator;

wherein each of said applications performs a function call to obtain a sequence number, said function call invoking a sequence number routine of a sequence number device that communicates a sequence number request to said primary sequence generator, said primary sequence number generator monotonically generating a sequence number in response to said request and communicating said generated sequence number to said secondary sequence number generator, said secondary sequence number generator storing said generated sequence number and forwarding said generated sequence number to said originating sequence number device, said originating sequence number device returning said generated sequence number in response to said function call.

22. (Previously Presented) The distributed computing system of claim 21 wherein said originating sequence number device performs a direct memory access to return said generated sequence number.

23. (Previously Presented) The distributed computing system of claim 21 wherein a processor executing an application that has performed said function call is placed in a spin loop while waiting for said generated sequence number to be returned.

24. (Previously Presented) The distributed computing system of claim 21 wherein an application performing said function call is placed in a sleep state when said generated sequence number is not received within a predetermined period of time.

25. (Previously Presented) The distributed computing system of claim 21 wherein a management process, executed on a processor of said plurality of nodes, configures said sequence number devices to select said primary and secondary sequence number generators.

26. (Previously Presented) The distributed computing system of claim 25 wherein, when said management process detects a failure of said primary sequence number generator, said management process selects said secondary sequence number generator to serve as a new primary sequence number generator.

27. (Previously Presented) The distributed computing system of claim 25 wherein said management process communicates an identity of said new primary sequence number generator to said sequence number devices of said plurality of nodes.